measured from said top surface of said epitaxial layer, to a first depth d_{max} at a first location and to a depth of d at a second location, where d is less than d_{max}, said first and second locations being separated by a predetermined horizontal distance;

a source region of said first conductivity type formed in said expitaxial layer above a portion of said body region, said portion of said body region being located between said second location and said source region; and

a trench formed in said epitaxial layer, having substantially vertical side walls, extending from said top surface of said epitaxial layer to a depth d_{tr}, said depth d_{tr} being less than said depth d_{max}, and greater than said depth d, said trench being (i) closer to said second location than said first location, and (ii) horizontally adjacent said source region;

wherein breakdown in said trench DMOS transistor occurs across said epitaxial layer at a position closer to said first location than said second location.

30. (Three times amended) A trench DMOS transistor cell, comprising:

a substrate of semiconductor material of a first electrical conductivity type having a top surface;

a first covering layer of semiconductor material of said first electrical conductivity type, said first covering layer (i) having a dopant concentration less than that of said substrate, (ii) having a top surface and (iii) being contiguous to and overlying the substrate top surface;

a second covering layer of semiconductor material of second electrical conductivity type having a top surface and being contiguous to the top surface of the first

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

covering layer and extending vertically downward from the top surface of the first covering layer into an upper portion of the first covering layer;

a third covering layer of semiconductor material of said first electrical conductivity type having a top surface and being contiguous to and partly overlying the top surface of the second covering layer, where the maximum depth of the second covering layer relative to the top surface of the third covering layer is a depth d_1;

a trench, having side walls and a bottom wall, said side walls extending vertically downward from the top surface of the third covering layer through the third and second covering layers and through a portion of, but not all of, the first covering layer, where the trench has a maximum depth relative to the top surface of the third covering layer equal to a second depth d_2 and d_2 is less than d_1;

a layer of oxide positioned within the trench and contiguous to the bottom walls and side walls of the trench so that portions [, but not all,] of the trench are filled with the oxide layer;

electrically conducting semiconductor material, contiguous to the oxide layer and positioned within the trench so that the oxide layer lies between the electrically conducting semiconductor material and the bottom and side walls of the trench; and

three electrodes that are electrically coupled to the electrically conducting semiconductor material in the trench, to the third covering layer and to the substrate, respectively;

wherein [the difference d_1-d_2 of said first and second depths d_1 and d_2 is sufficient to force] junction breakdown occurs away from the trench and into [the heavily doped] a portion of the second covering layer.

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979